

945G- M6

Rev: A

Page Title of Schematic :

Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	35		02/02/' 05
B	B	35		03/22/' 05
1.0	1.0	35		05/22/' 05
A	A	35		11/05/' 05

Title	Page	Title	Page
Cover Sheet	1		
System Block Diagram	2		
P4 LGA775P Part A	3		
P4 LGA775P Part B	4		
P4 LGA775P Part C	5		
P4 LGA775P Part D	6		
P4 LGA775P Part E	7		
Clock Generator(CK410)	8		
I-LP(MCH)Part A & E & F	9		
I-LP(MCH)Part D	10		
I-LP(MCH)Part B & C	11		
I-LP(MCH)Part G	12		
DDIMM 1&2 (DDR SDRAMs)	13		
DDIMM 3&4 (DDR SDRAMs)	14		
DDR & V_FSB_VTT Power	15		
PCI EXPRESS 16-PORT	16		
ICH7 Part A & D (SATA-CONNECTOR)	17		
ICH7 Part B & C (RTC)	18		
ICH7 Part E & F (POWER & GND)	19		
IDE1 Connector	20		
USB/FWH	21		
LPC_FDD/KB/M	22		
I/O Ports	23		
H/W Monitor	24		
Azalia Codec	25		
Audio Interface	26		
ATX Power & Front Panel	27		
LAN	28		
Vcore DC-DC	29		
MIS DC-DC(DUAL & VDDQ)	30		
PCI Slot 1&2	31		
PCI Slot 3 & PCI Extender	32		
Back I/O	33		
VT6307 (1394)	34		
Schematic Change History	35		

DEVICE	IDSEL	INT#	REQ#	GN#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	D	PREQ-3	PGNT-3
LAN	21	E	PREQ-4	PGNT-4
EPCI1	22	A/B/C/D	PREQ-5	PGNT-5
EPCI2	23	B/C/D/A	PREQ-5	PGNT-5

PCB : 244 x 244 mm ; 4 layers

BW : 4.1GB/s @ FSB : 533MHz & Freq : 133MHz
BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz
BW : 6.4GB/s @ FSB : 1066MHz & Freq : 266MHz

INTEL
P4 Processor
PSC, Smithfield -
LGA 775 pin



INTEL
i945G/P
1210pin FC-BGA

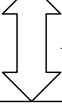
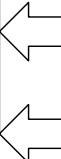
BW : 10.7GB/s @ DDR2 :533/667MHz

DDIMM1: DDR2 Socket 240P

DDIMM2 : DDR2 Socket 240P

DDIMM3: DDR2 Socket 240P

DDIMM4 : DDR2 Socket 240P



BW : 2GB/s (Support Lsoch)

INTEL
ICH7
652pin EBGA

PCIEx1

BW : 133MB/s @ Freq : 33MHz

PCI1 Slot 120pin @ AD17

PCI2 Slot 120pin @ AD18

PCI3 Slot 120pin @ AD19

PCI4 Slot 120pin @ AD22

PCI5 Slot 120pin @ AD23



USB V2.0

USB1 2 ports
USB2 2 ports
USB3 2 ports
USB4 2 ports

Up to Ultra ATA/100

IDE1 40pin

One IDE Channel

Azalia I/F

Audio Codec
ALC882

Line in
Line out
Mic in
Center/Bass out
Surround
Side-Surround

SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin

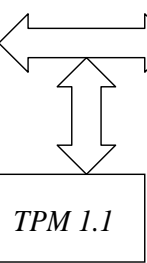
BW : 150MB/s

intel
FWH
32pin PLCC

TPM 1.1

LPC bus

Super I/O
ITE8712
128pin PQFP

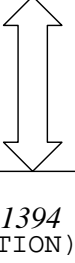


VIA 1394
(OPTION)

10/100
Lan

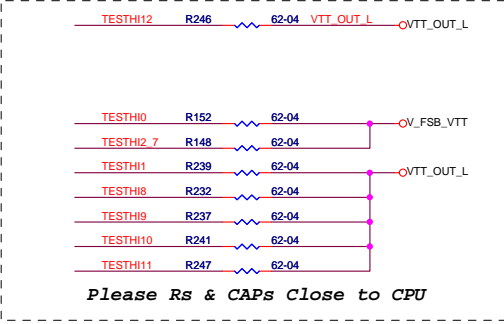
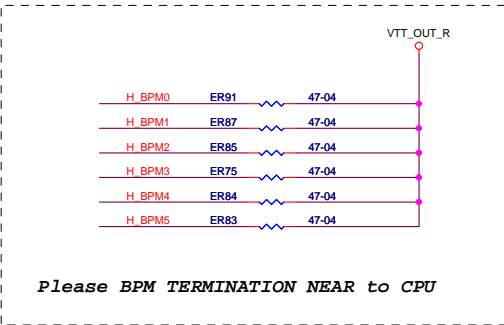
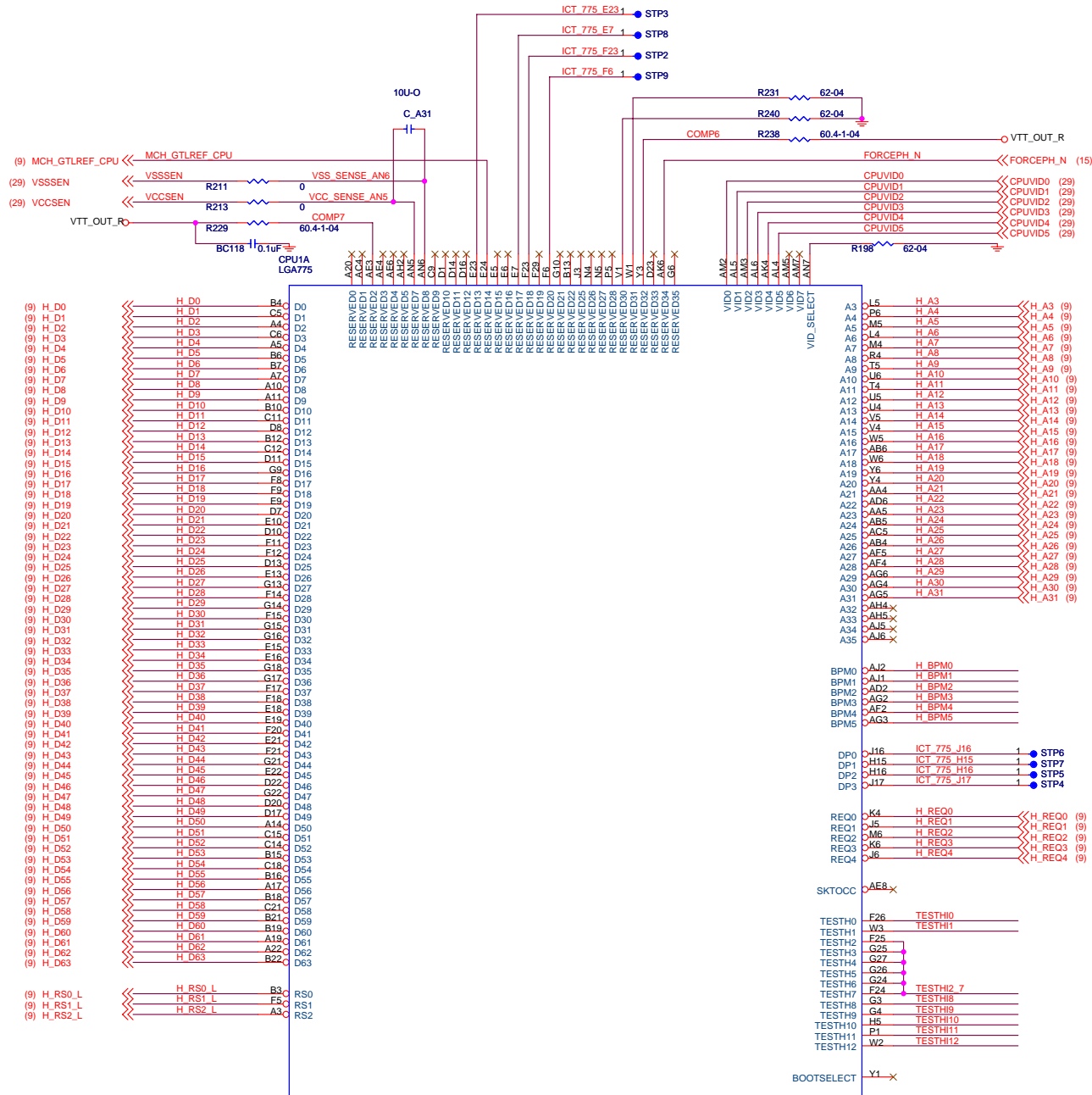
USBLAN
RJ45

CONN/
HEADER

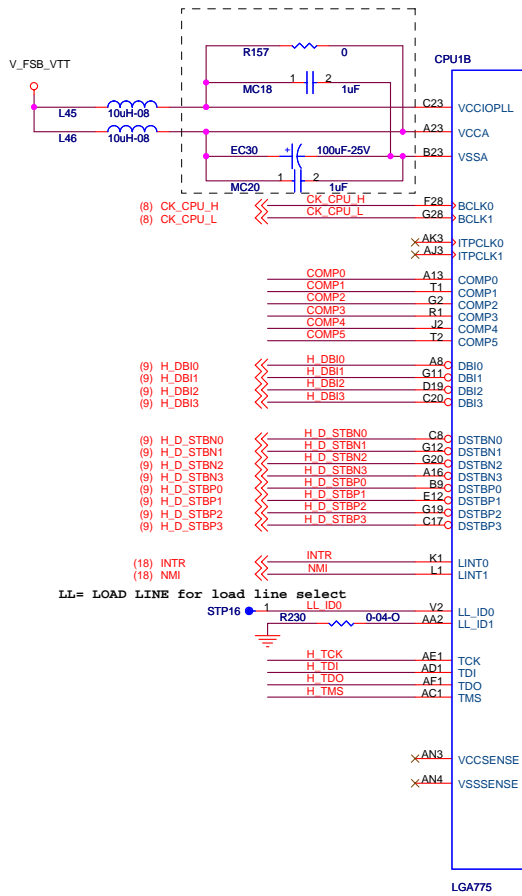


Elitegroup Computer Systems

Title System Block Diagram		
Size B	Document Number 945G-M6	Rev A
Date: Friday, November 11, 2005	Sheet 2	of 35



Place componets as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils



LL= LOAD LINE for load line select

STP16 1

R230 0-04-0 AA2

V2 LL_ID0 LL_ID1

H TCK AE1 TCK

H TDI AE1 TDI

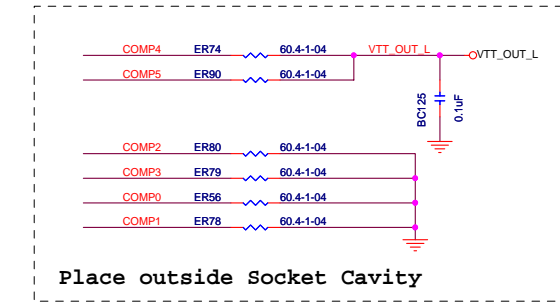
H TDO AE1 TDO

H TMS AC1 TMS

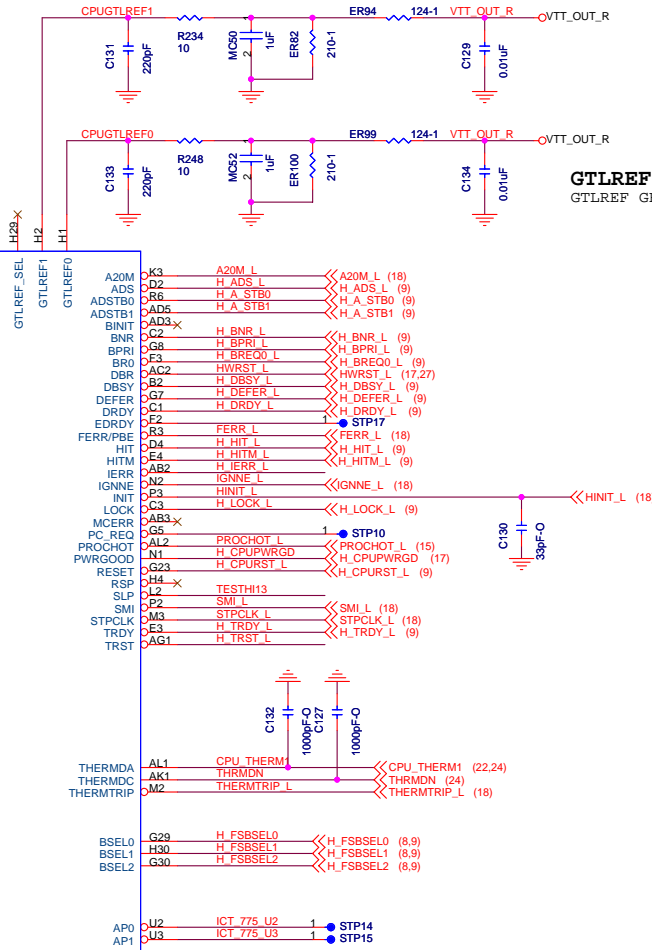
AN3 VCCSENSE

AN4 VSSSENSE

LGA775

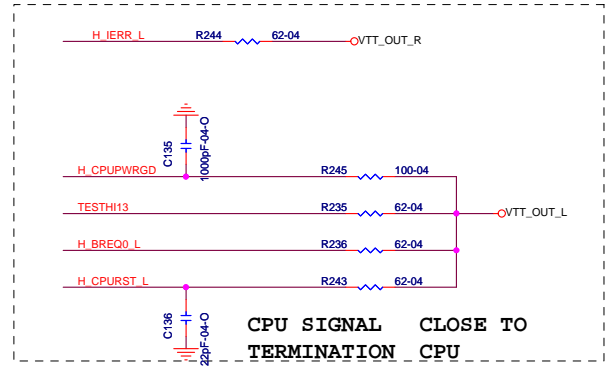


Place outside Socket Cavity

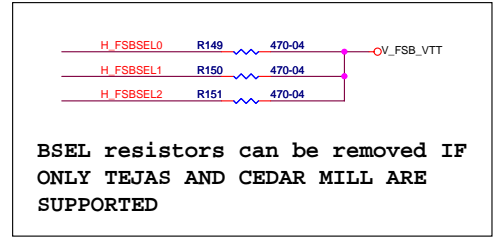


$$GTLREF = 0.67 * VTT = 0.8V$$

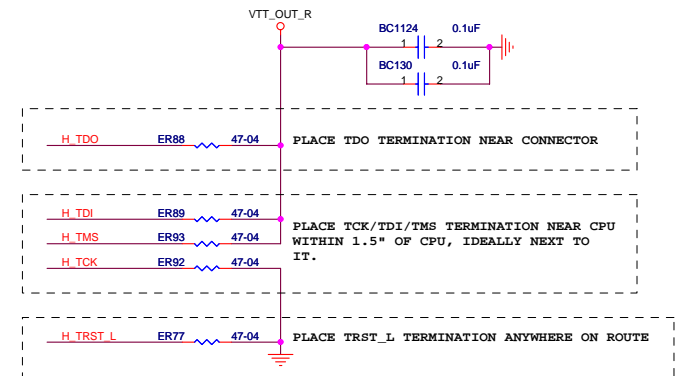
GTLREF GENERATION CIRCUITS



CPU SIGNAL CLOSE TO
TERMINATION CPU



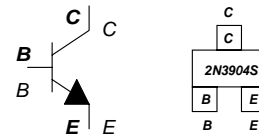
BSEL resistors can be removed IF
ONLY TEJAS AND CEDAR MILL ARE
SUPPORTED



PLACE TDO TERMINATION NEAR CONNECTOR

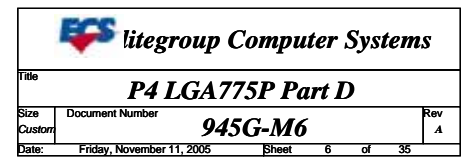
PLACE TCK/TDI/TMS TERMINATION NEAR CPU
WITHIN 1.5" OF CPU, IDEALLY NEXT TO
IT.

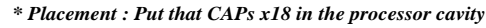
PLACE TRST_L TERMINATION ANYWHERE ON ROUTE



P4 LGA775P Part B			
945G-M6			
Title Size Custom	Document Number Date: Friday, November 11, 2005	Sheet 4 of 35	Rev A







The diagram shows three capacitors, SC1, SC2, and SC3, connected in parallel. The positive terminal (P) of each capacitor is connected to a common node labeled VCCP. The negative terminal (N) of each capacitor is connected to a common ground symbol. Each capacitor is labeled with its value and specifications: 100uF-2V-SP.

CPU1E LGA775

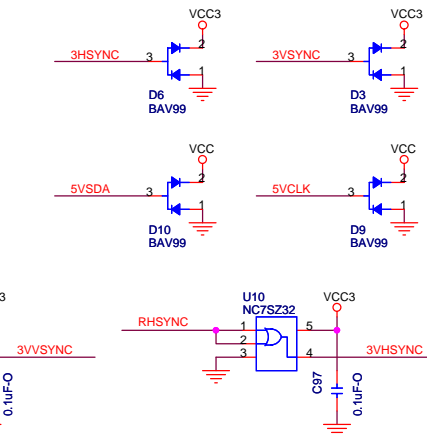
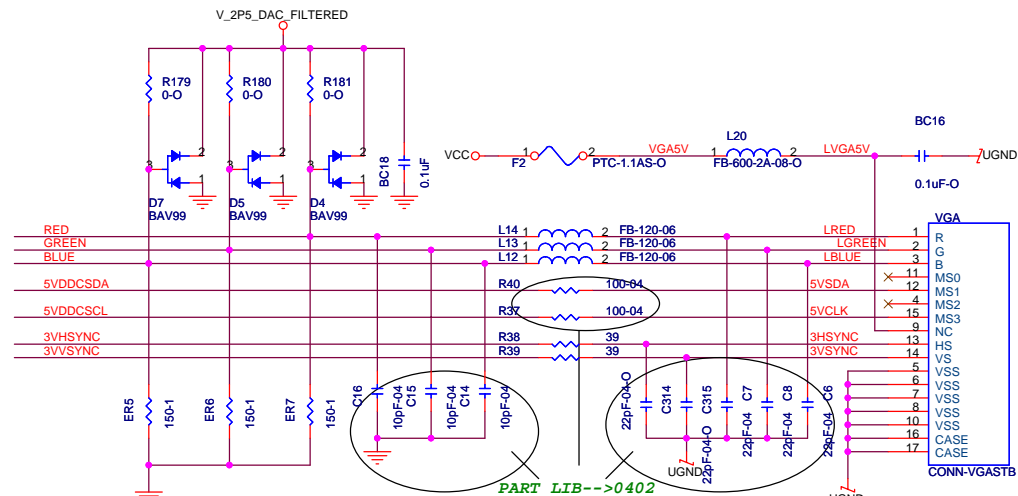
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_SEL
VTT_PWRGD

V_FSB_VTT

VTT0
VTT1
VTT2
VTT3
VTT4
VTT5
VTT6
VTT7
VTT8
VTT9
VTT10
VTT11
VTT12
VTT13
VTT14
VTT15
VTT16
VTT17
VTT18
VTT19
VTT20
VTT21
VTT22
VTT23

AA1
J1
F27
AM6
A25
A26
A27
A28
A29
A30
B25
B26
B27
B28
B29
B30
C25
C26
C27
C28
C29
C30
D25
D26
D27
D28
D29
D30

STP1 ● 1
 (29) PWR_GD << PWR_GD



100nH/S/1.4A/台慶 (FPG0302-R10M-01)

V_1P5_PCIEXPRESS

L55

0.1uH-12

VDD0

MC48 100F/10V-08

MC49 100F/10V-08

MC50 100F/10V-08

C11 100F/10V-08

C12 100F/10V-08

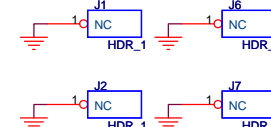
C13 100F/10V-08

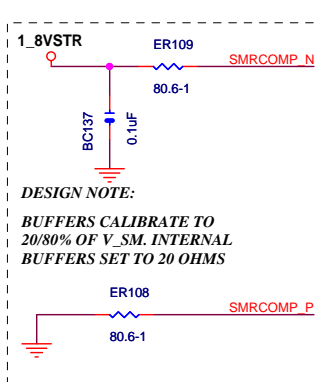
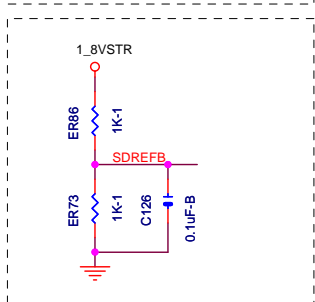
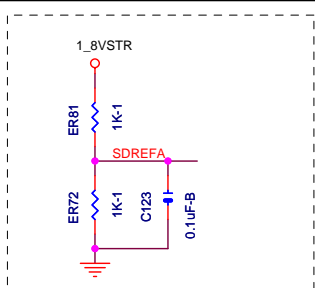
SC7 100F/10V-08

PCI EXPRESS FILTER

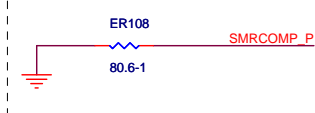
CAPS FOR SPECIFIC CORE MCH

Figure 10 illustrates the termination for the PCIE2.0 signal lines. The diagram shows three signal lines (EXP_SLR, EXP_EN, EXP_GRCOMP) and their termination components (R169, R172, SR1). It also shows the termination of the COMP SIGNAL TERMINATION (SC12, SC11, R164, R163) and the termination of the PWROK, PLTRST_L, GHSYNC, and GVSIGNAL lines (R145, R158, R140, R141, R146, R159, R160, R161).

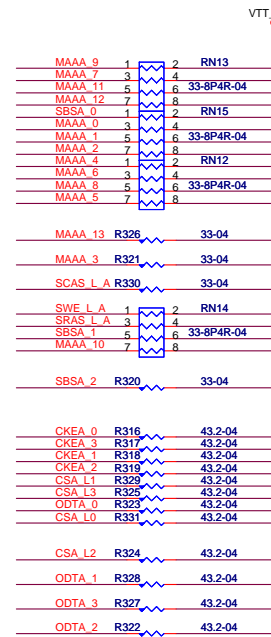
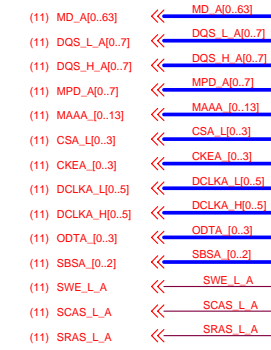
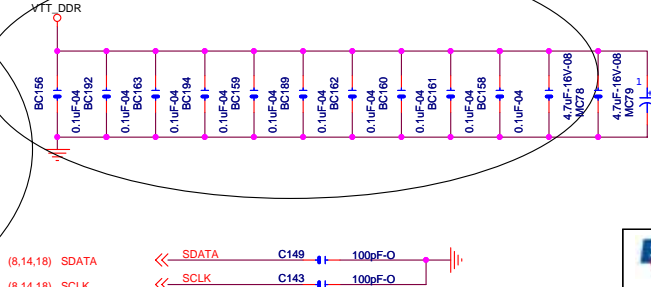
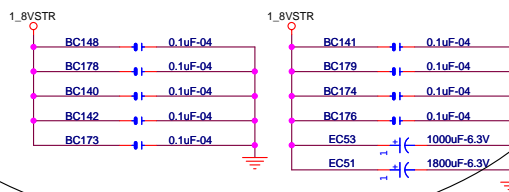
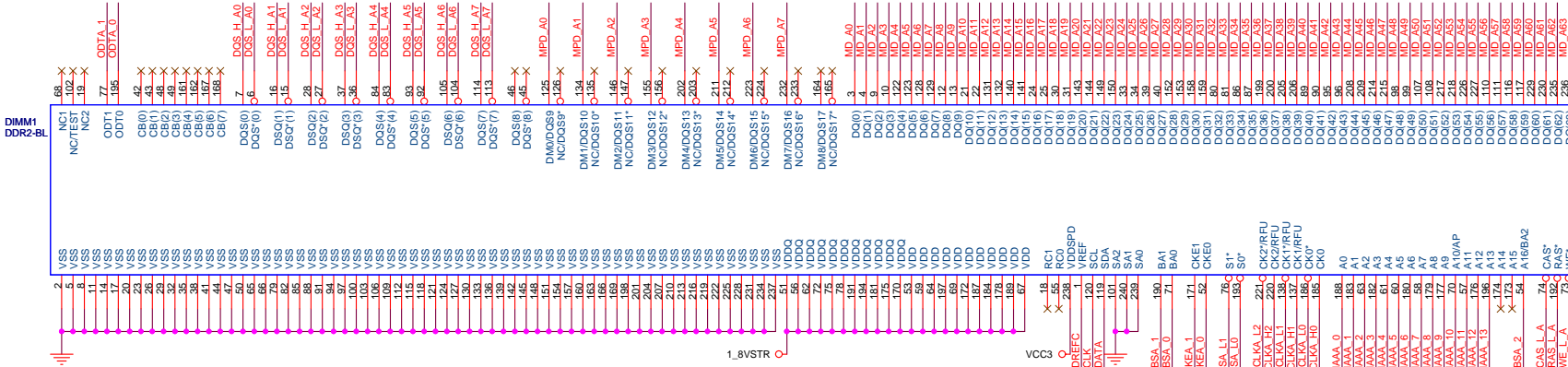
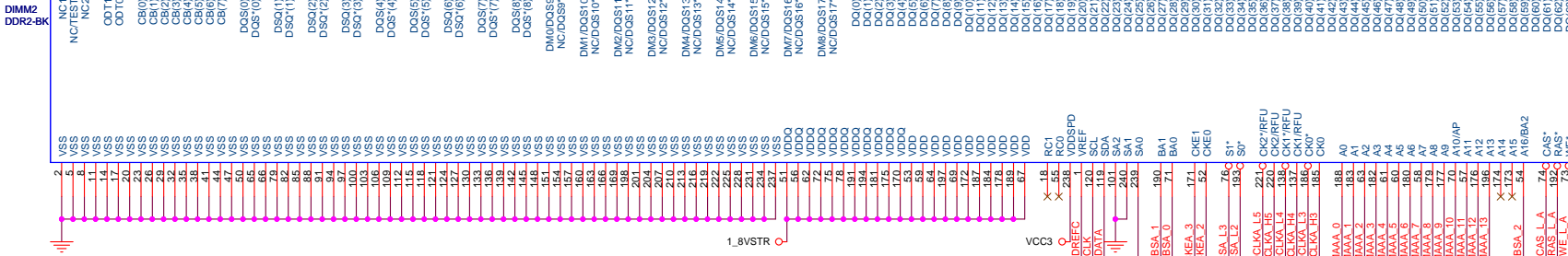
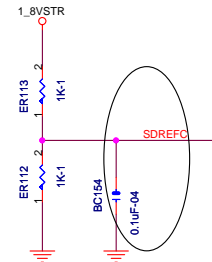




DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_{SM} INTERNAL
BUFFERS SET TO 20 OHMS



		U13C LAKEPORT
DOS_H_A4	AU35	SDQS_A4
DOS_L_A4	AV35	#SDQS_A4
MPD_A4	AT34	SDM_A4
MD_A32	AP32	SDQ_A32
MD_A33	AV34	SDQ_A33
MD_A34	AV38	SDQ_A34
MD_A35	AU39	SDQ_A35
MD_A36	AV32	SDQ_A36
MD_A37	AT32	SDQ_A37
MD_A38	AR34	SDQ_A38
MD_A39	AU37	SDQ_A39
DOS_H_A5	AP42	SDQS_A5
DOS_L_A5	AP40	#SDQS_A5
MPD_A5	AP39	SDM_A5
MD_A40	AR41	SDQ_A40
MD_A41	AR42	SDQ_A41
MD_A42	AN43	SDQ_A42
MD_A43	AM40	SDQ_A43
MD_A44	AU41	SDQ_A44
MD_A45	AU42	SDQ_A45
MD_A46	AP41	SDQ_A46
MD_A47	AN40	SDQ_A47
DOS_H_A6	AG42	SDQS_A6
DOS_L_A6	AG41	#SDQS_A6
MPD_A6	AG40	SDM_A6
MD_A48	AL41	SDQ_A48
MD_A49	AL42	SDQ_A49
MD_A50	AF39	SDQ_A50
MD_A51	AE40	SDQ_A51
MD_A52	AM41	SDQ_A52
MD_A53	AM42	SDQ_A53
MD_A54	AF41	SDQ_A54
MD_A55	AF42	SDQ_A55
DOS_H_A7	AC42	SDQS_A7
DOS_L_A7	AC41	#SDQS_A7
MPD_A7	AC40	SDM_A7
MD_A56	AD40	SDQ_A56
MD_A57	AD43	SDQ_A57
MD_A58	AA39	SDQ_A58
MD_A59	AA40	SDQ_A59
MD_A60	AE42	SDQ_A60
MD_A61	AE41	SDQ_A61
MD_A62	AB41	SDQ_A62
MD_A63	AB42	SDQ_A63
MAAA_0	BA32	SMA_A0
MAAA_1	AW32	SMA_A1
MAAA_2	BB30	SMA_A2
MAAA_3	BA30	SMA_A3
MAAA_4	AY30	SMA_A4
MAAA_5	BA27	SMA_A5
MAAA_6	BC28	SMA_A6
MAAA_7	AY27	SMA_A7
MAAA_8	AY28	SMA_A8
MAAA_9	BB27	SMA_A9
MAAA_10	AY33	SMA_A10
MAAA_11	AW27	SMA_A11
MAAA_12	BB26	SMA_A12
MAAA_13	BC38	SMA_A13
DCLKA_H0	BB32	SCLK_A0
DCLKA_L0	AY32	#SCLK_A0
DCLKA_H1	AY5	SCLK_A1
DCLKA_L1	BB5	#SCLK_A1
DCLKA_H2	AK42	SCLK_A2
DCLKA_L2	AK41	#SCLK_A2
DCLKA_H3	BA31	SCLK_A3
DCLKA_L3	BB31	#SCLK_A3
DCLKA_H4	AY6	SCLK_A4
DCLKA_L4	BA5	#SCLK_A4
DCLKA_H5	AH40	SCLK_A5
DCLKA_L5	AH43	#SCLK_A5
STP22	1	AL17
STP21	1	AK17
		RSVD_TP1
		RSVD_TP0



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Title: **DDIMM 1&2 (DDR SDRAMs)**

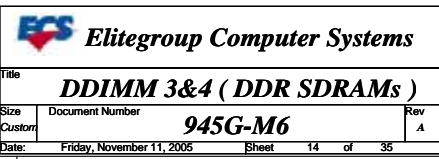
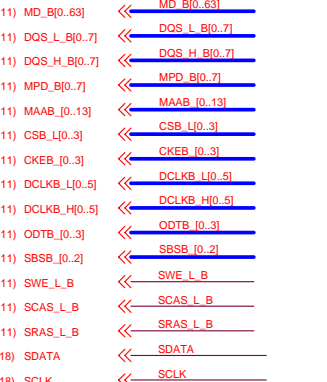
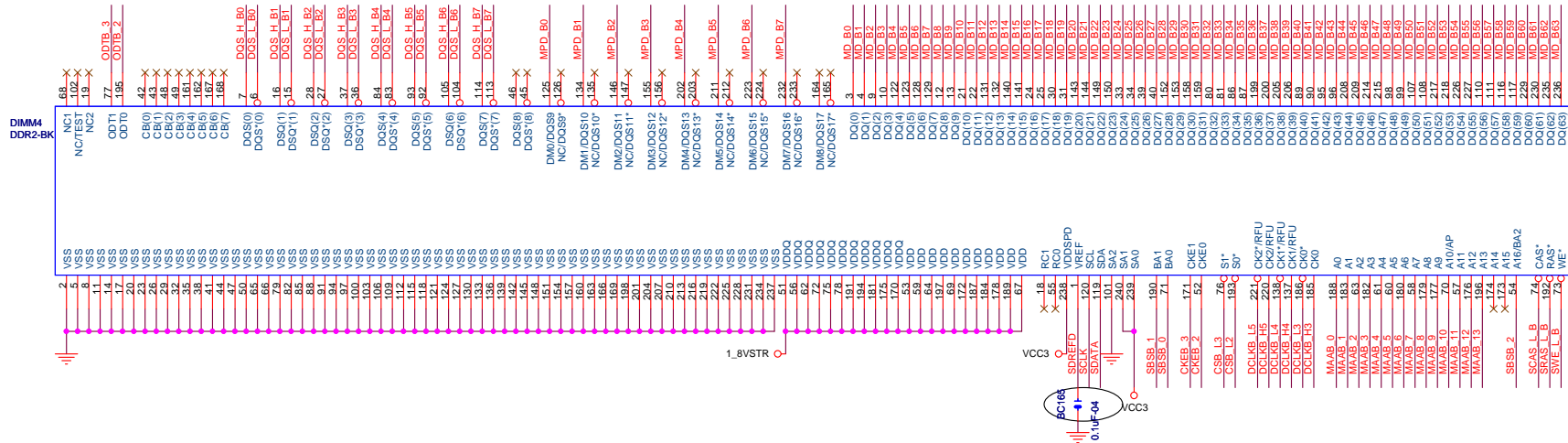
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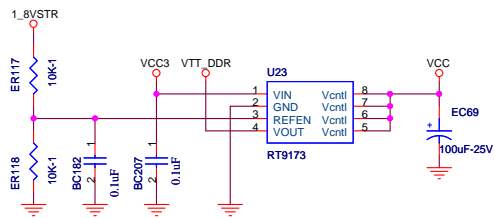
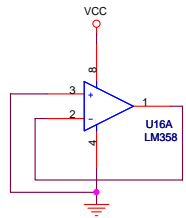
Customer: **945G-M6**

Date: **Friday, November 11, 2005**

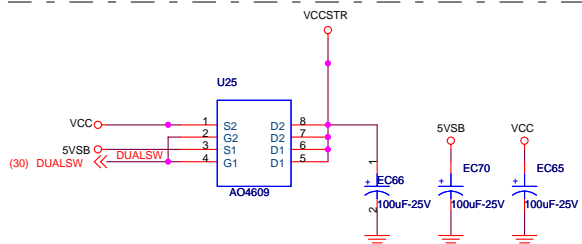
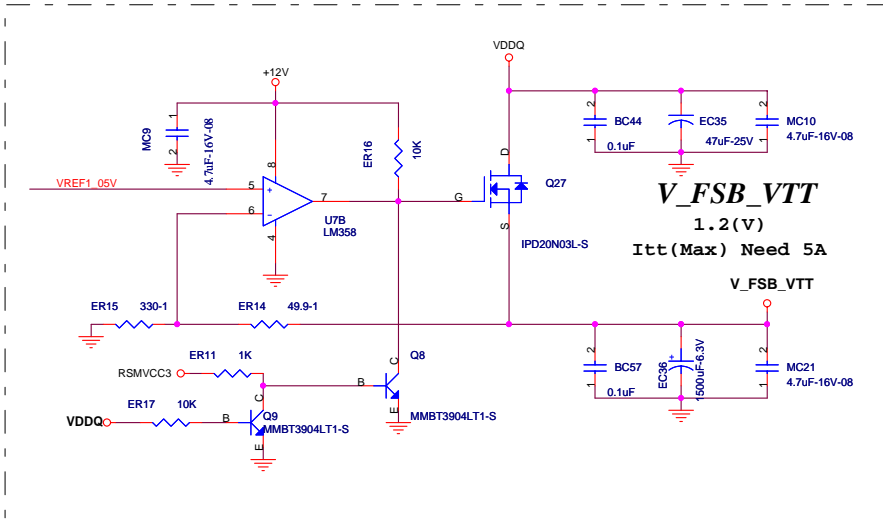
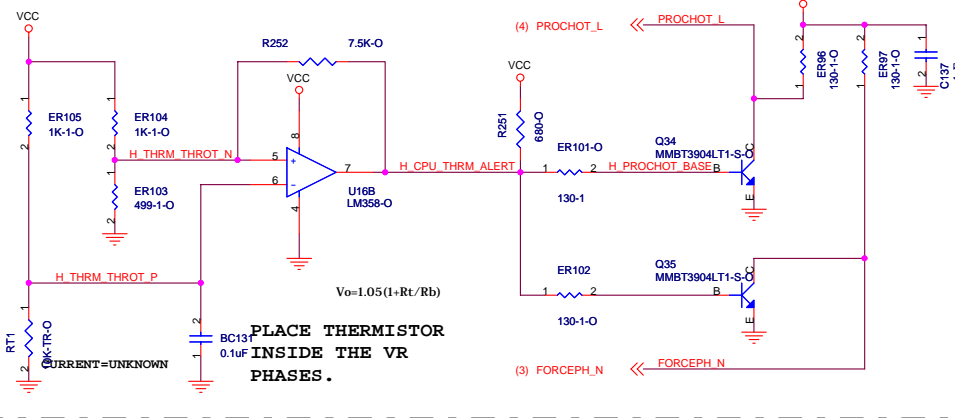
Sheet: **48** of **35**

Rev: **A**



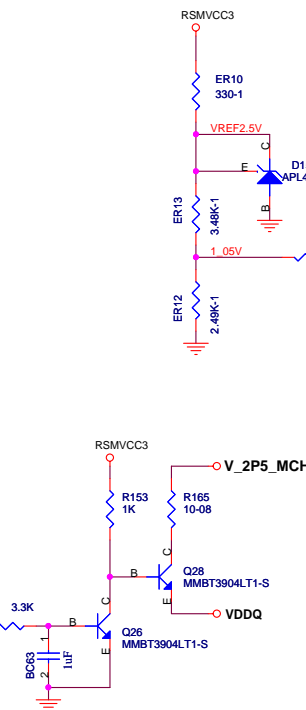


VR THERMAL THROTTLE CIRCUITRY



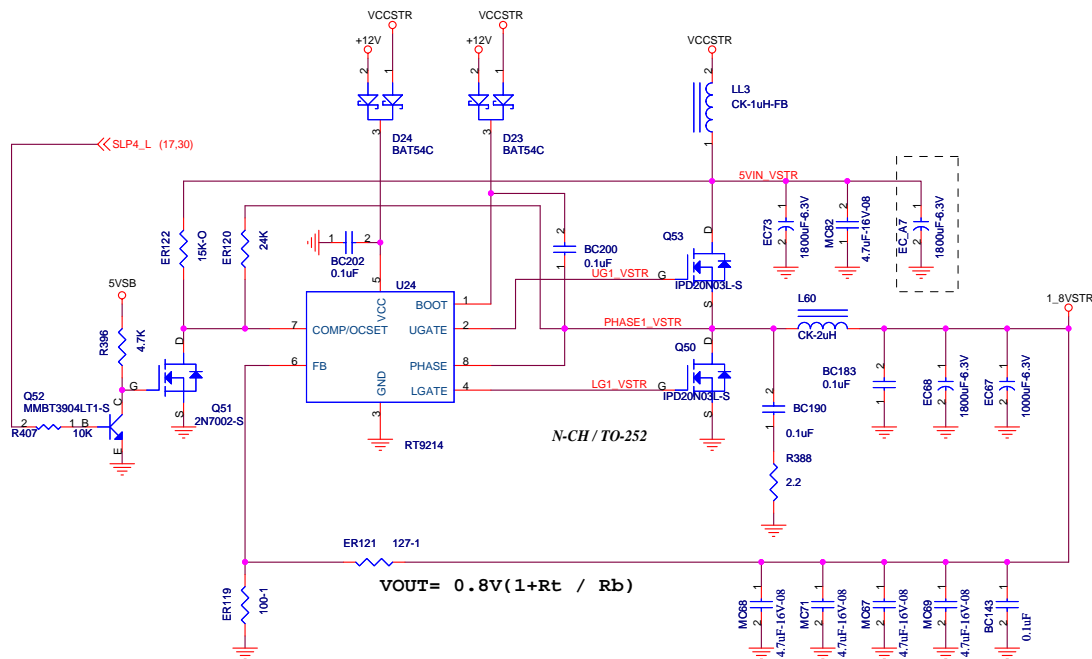
(17,22,30) SLP3_L

SLP4_L (17,30)



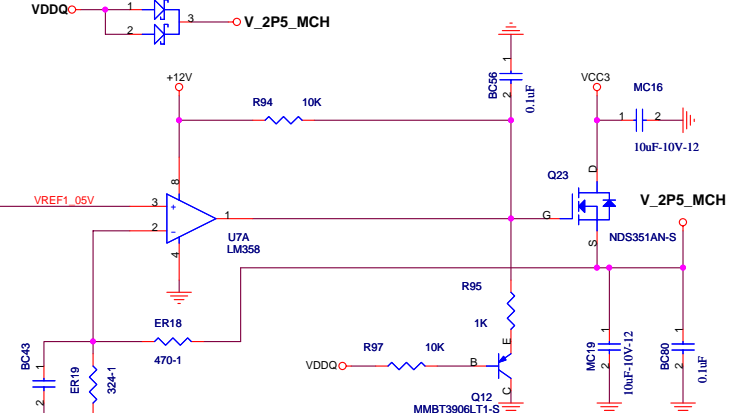
SLP4_L (17,30)

1.8VSTR should be able to support up to 14A

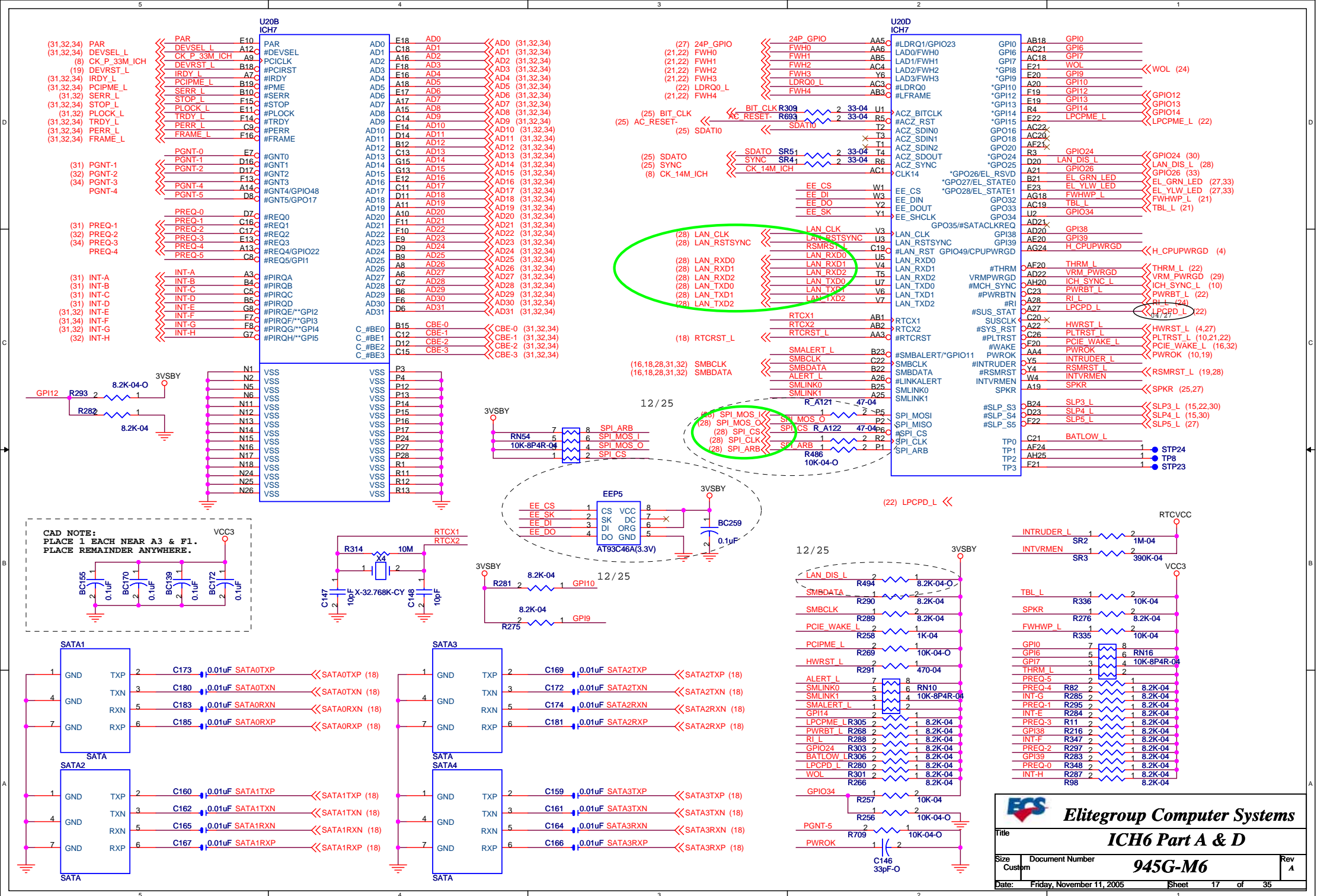


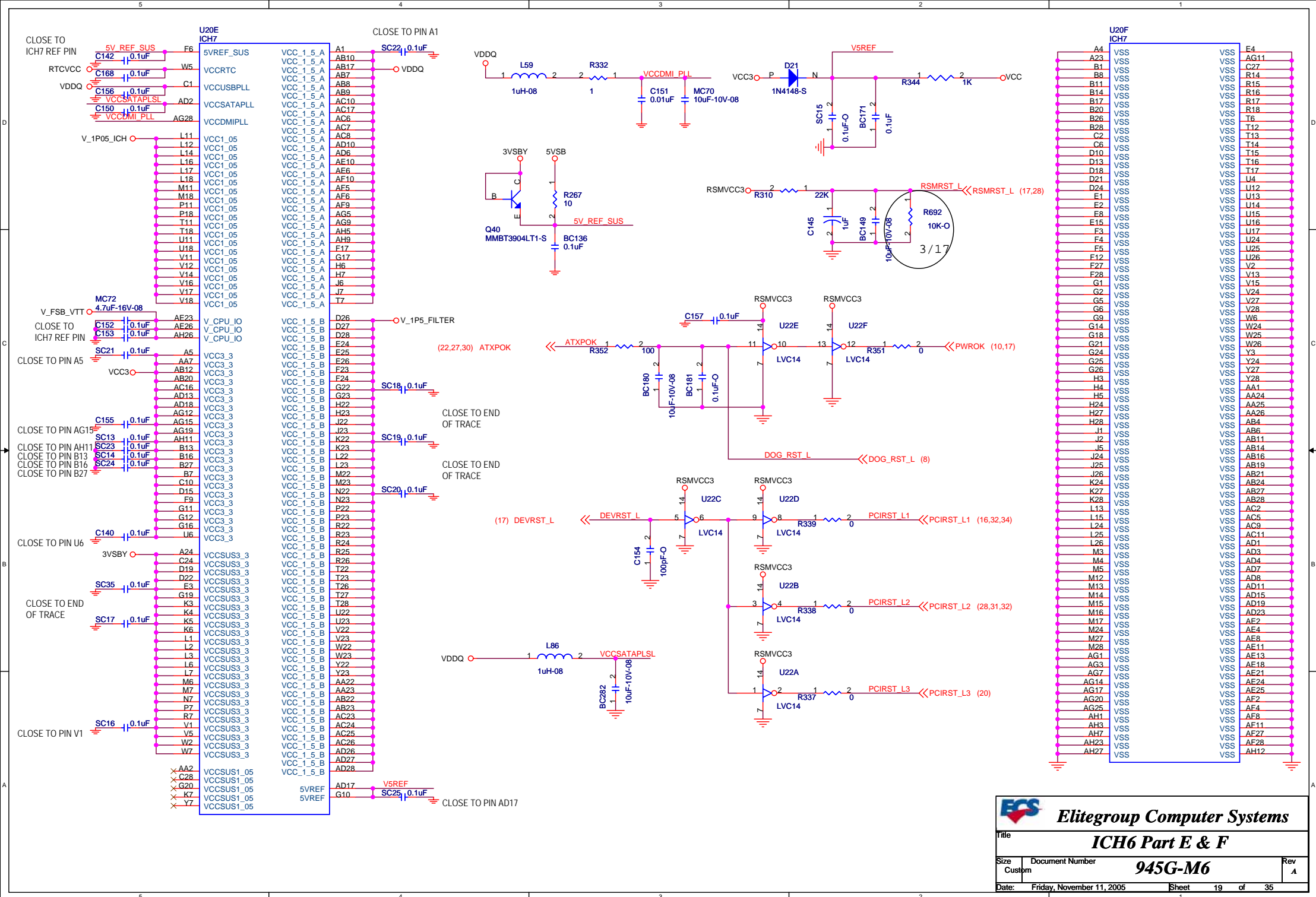
$VOUT = 0.8V(1 + R_t / R_b)$

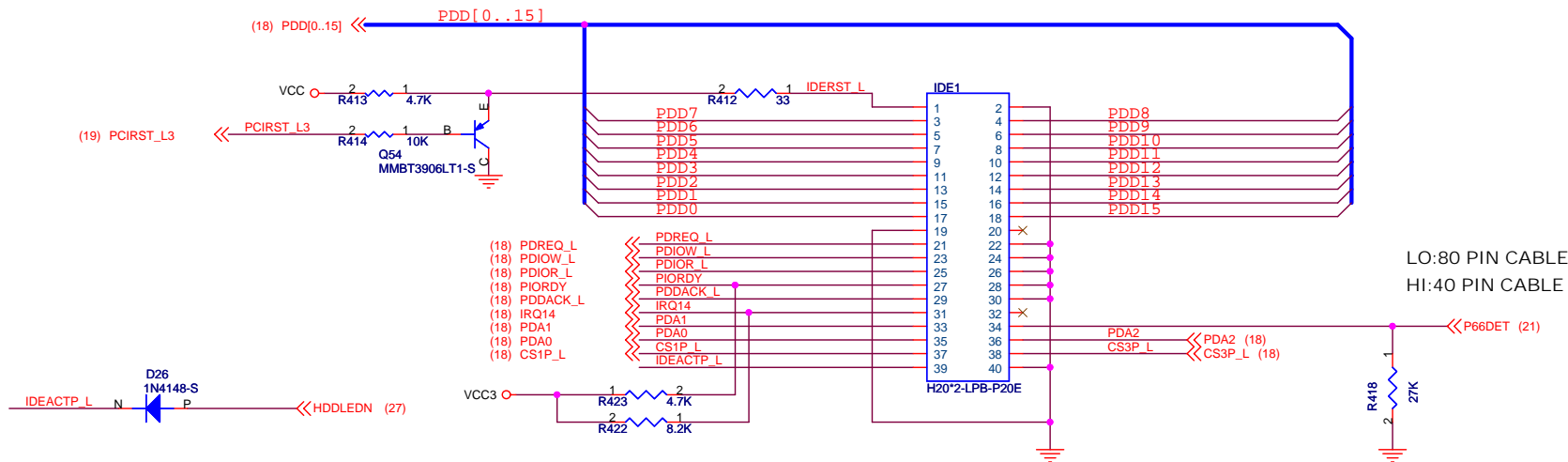
V_2P5_MCH



V_2P5_MCH(100mA)



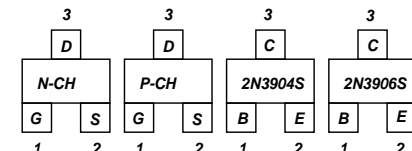
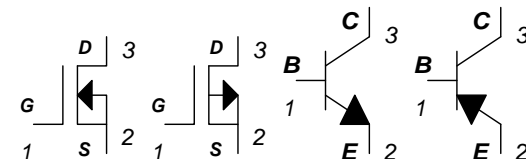




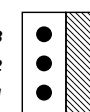
MAX TRACE LENGTH IS 8"

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

Top View SOT-23

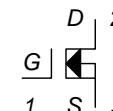


Fan Header

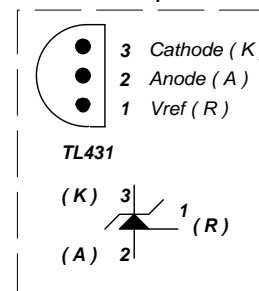


AMP640456-3

TO-263 / TO-252



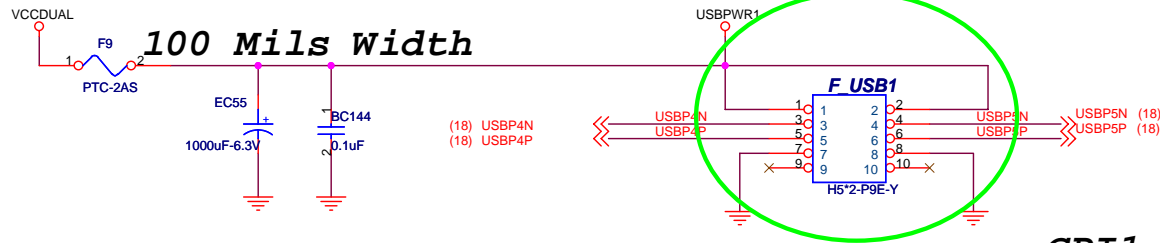
Top View



Elitegroup Computer Systems

Title		
IDE Connector		
Size	Document Number	Rev
Custom	945G-M6	A
Date:	Friday, November 11, 2005	Sheet 20 of 35

USB PORT INTERFACE



GPI1:

High:XXX Install

Low:XXX

GPI2:

High:1394 Install

Low:1394 xxx

GPI3:

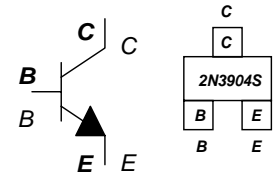
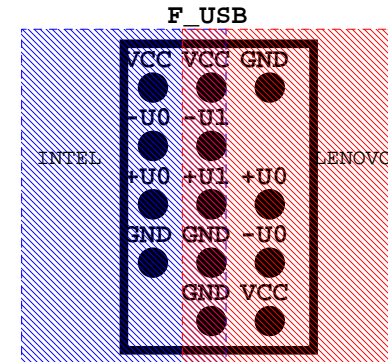
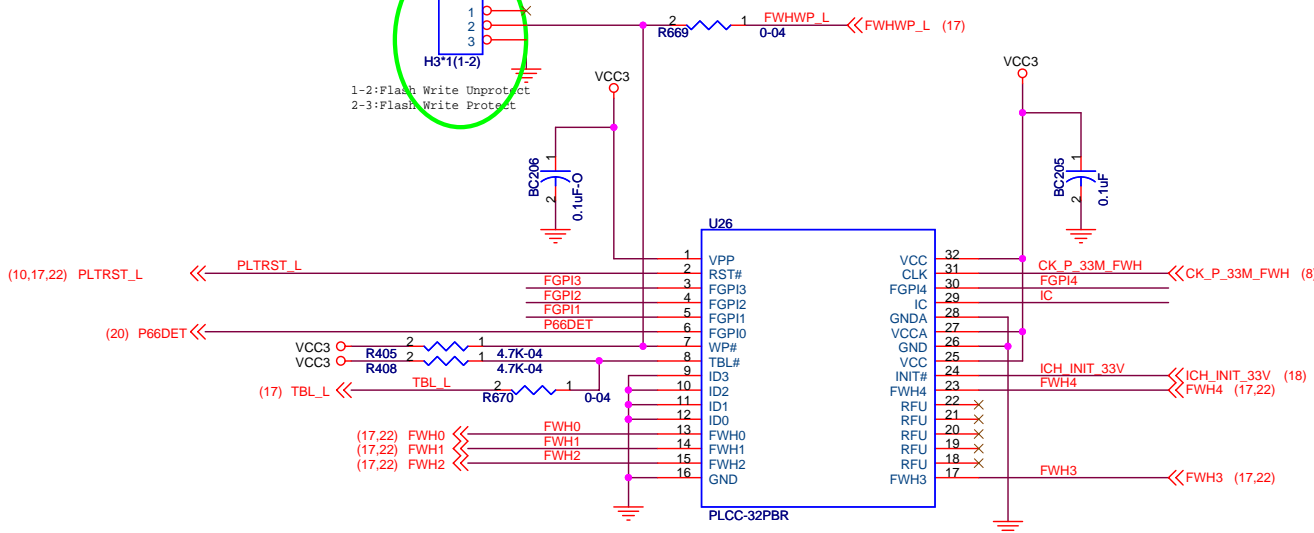
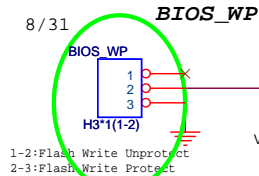
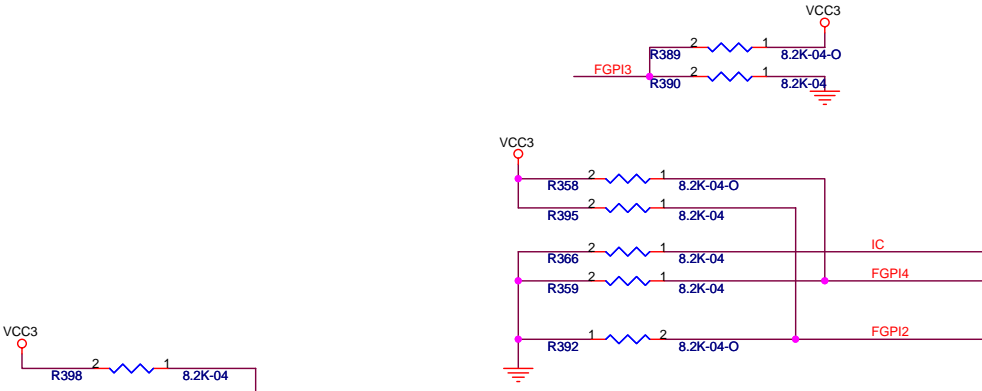
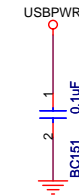
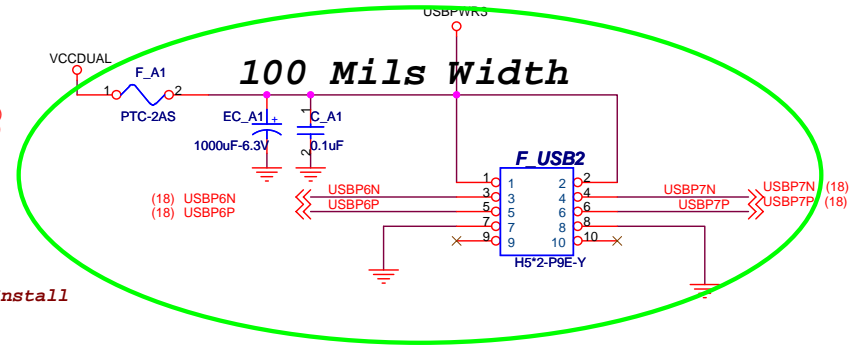
High:Suspend xxx

Low:suspend install

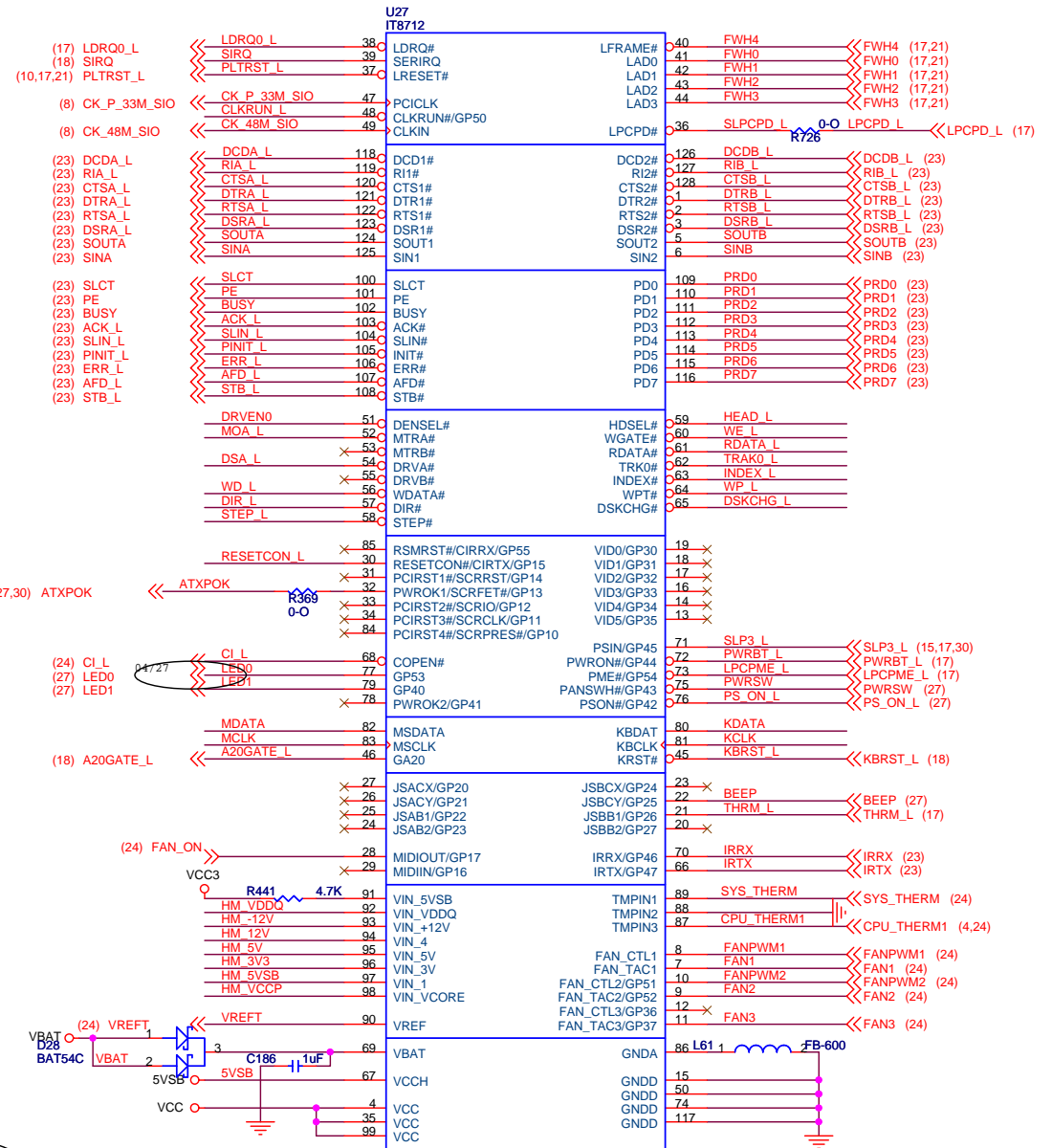
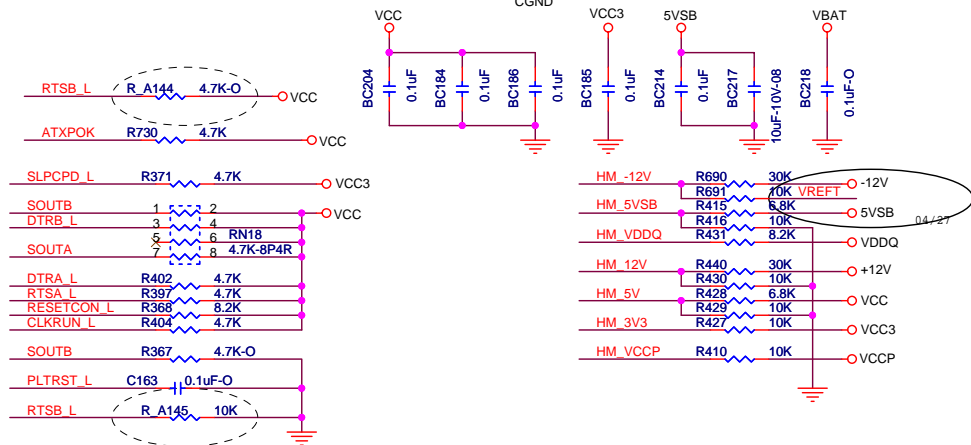
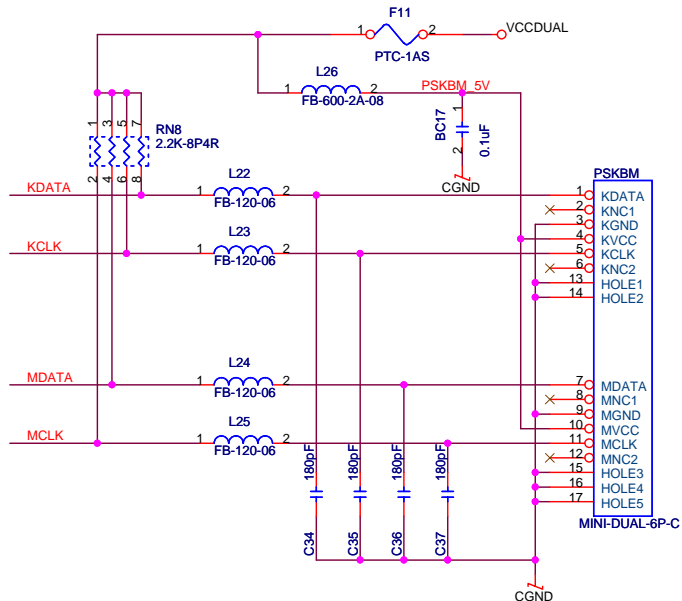
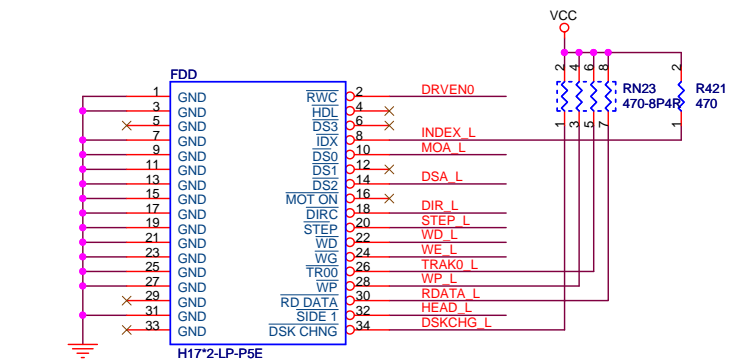
GPI4:

High:3-COM Lan Install

Low:Realtek PCI Lan install

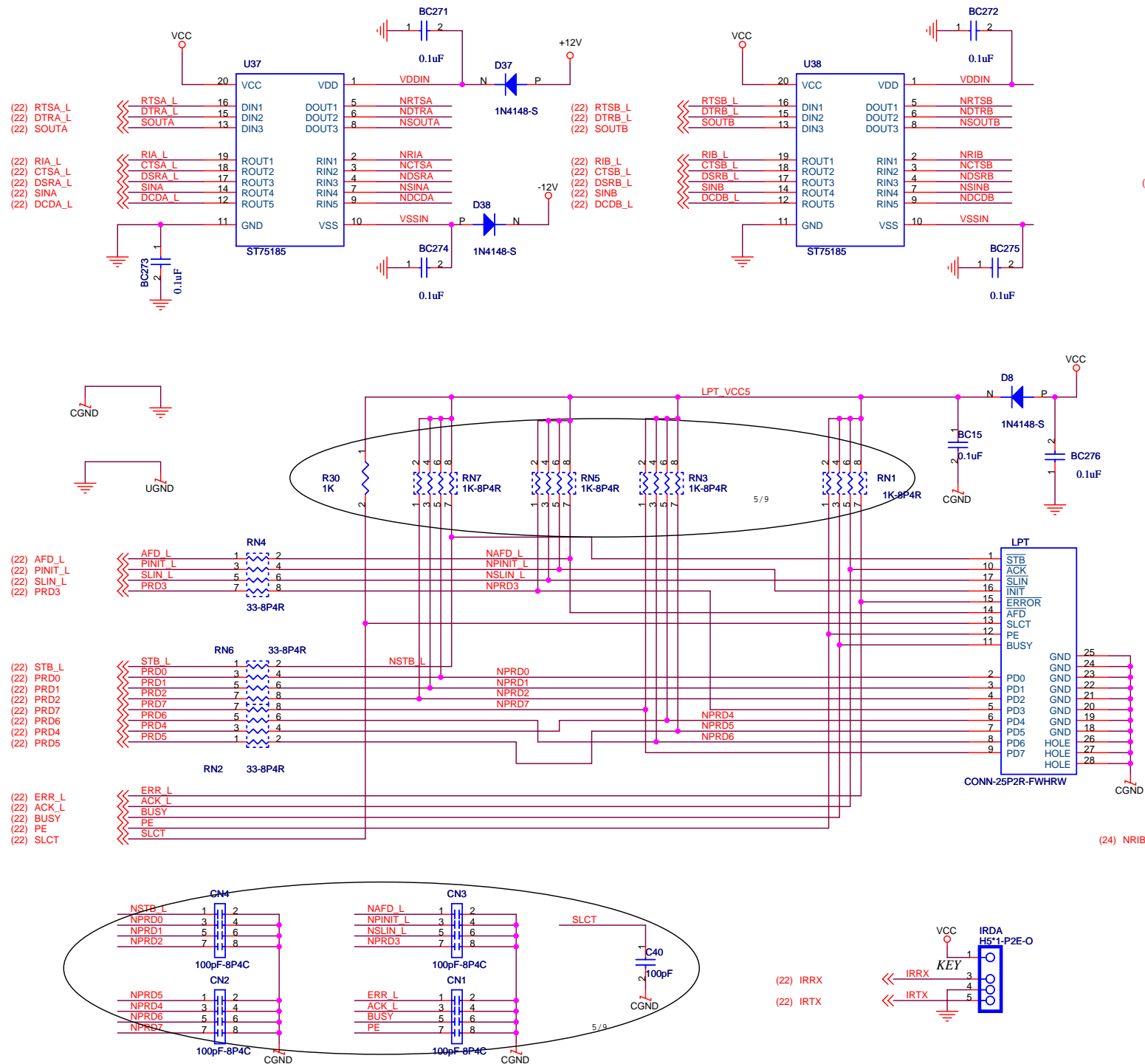


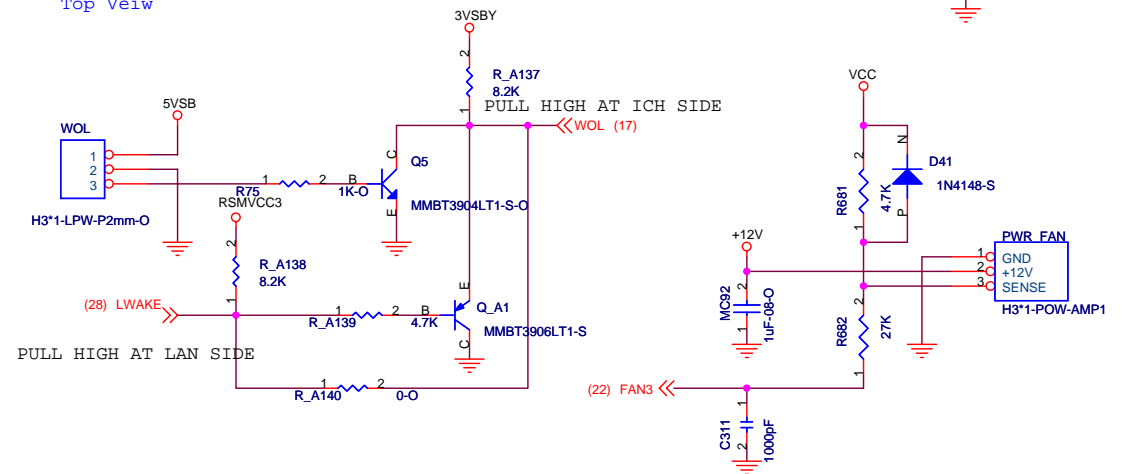
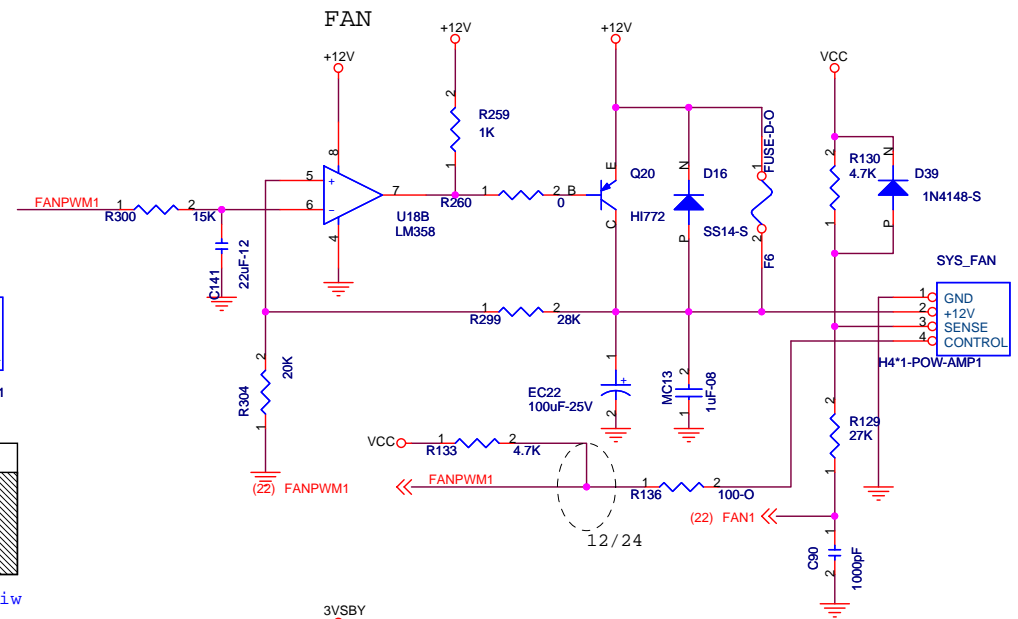
USB/FWH		
Title	Document Number	
Size	945G-M6	
Date:	Friday, November 11, 2005	Sheet 21 of 35

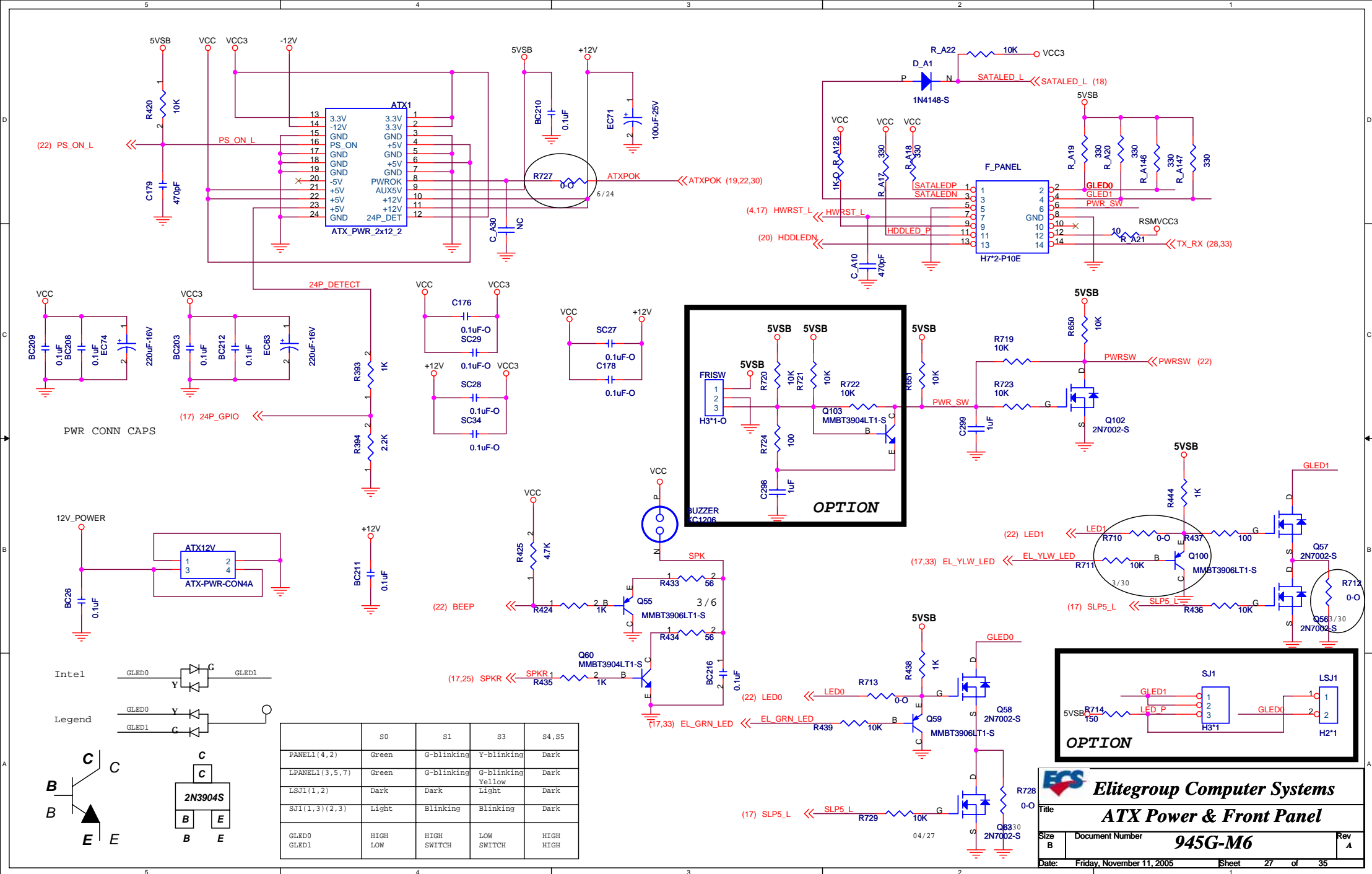


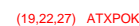
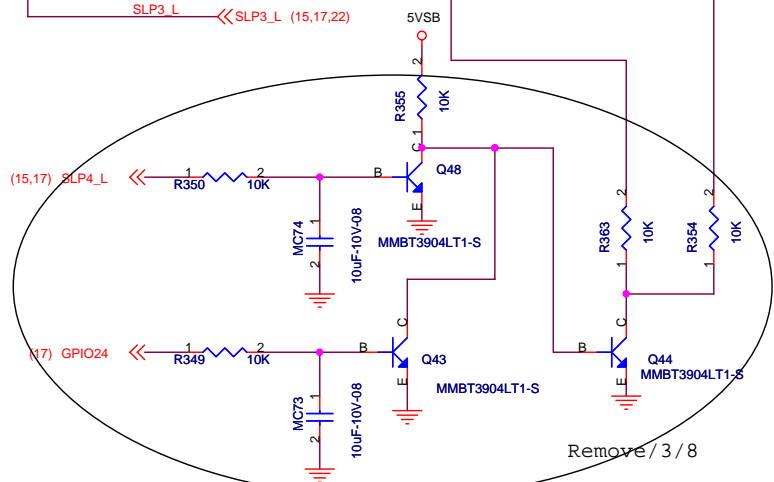
Elitegroup Computer Systems

Title			LPC_FDD/KB/M		
Size	Document Number	945G-M6			Rev
Custom					A
Date:	Friday, November 11, 2005	Sheet	22	of	35

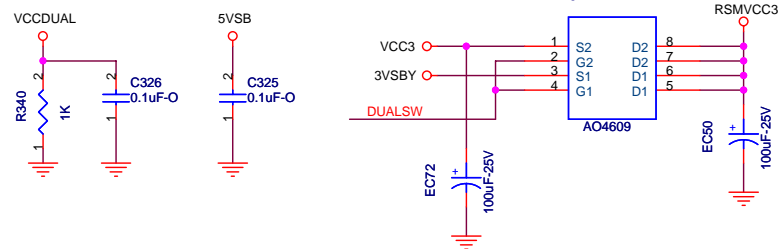
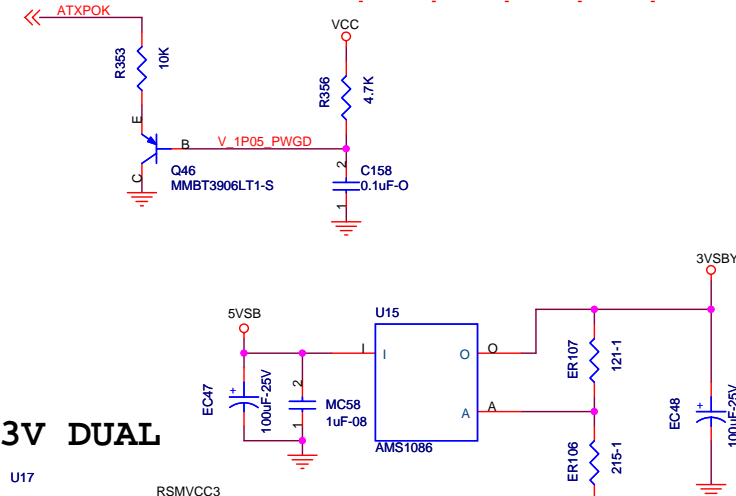


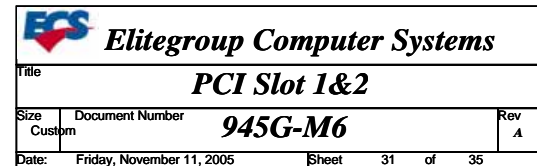


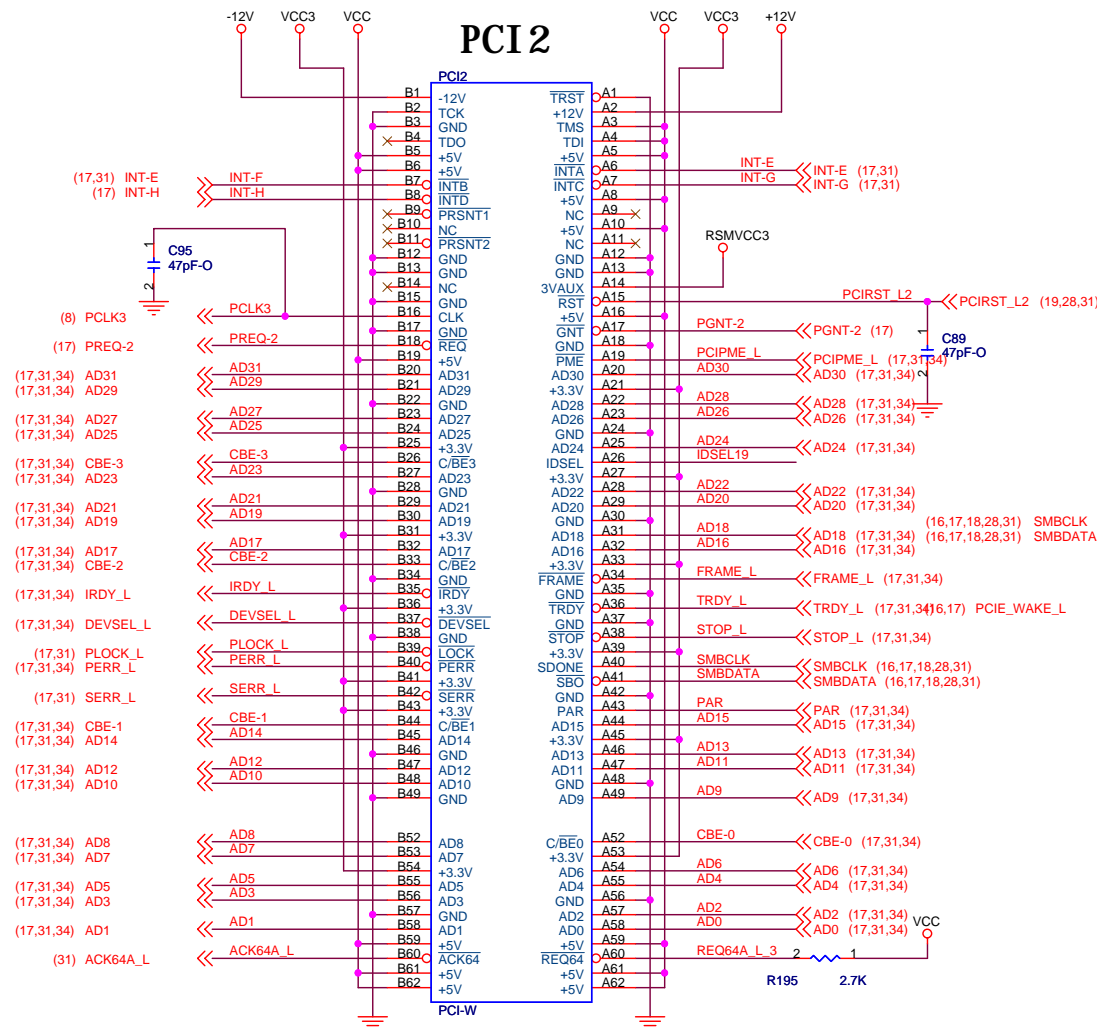




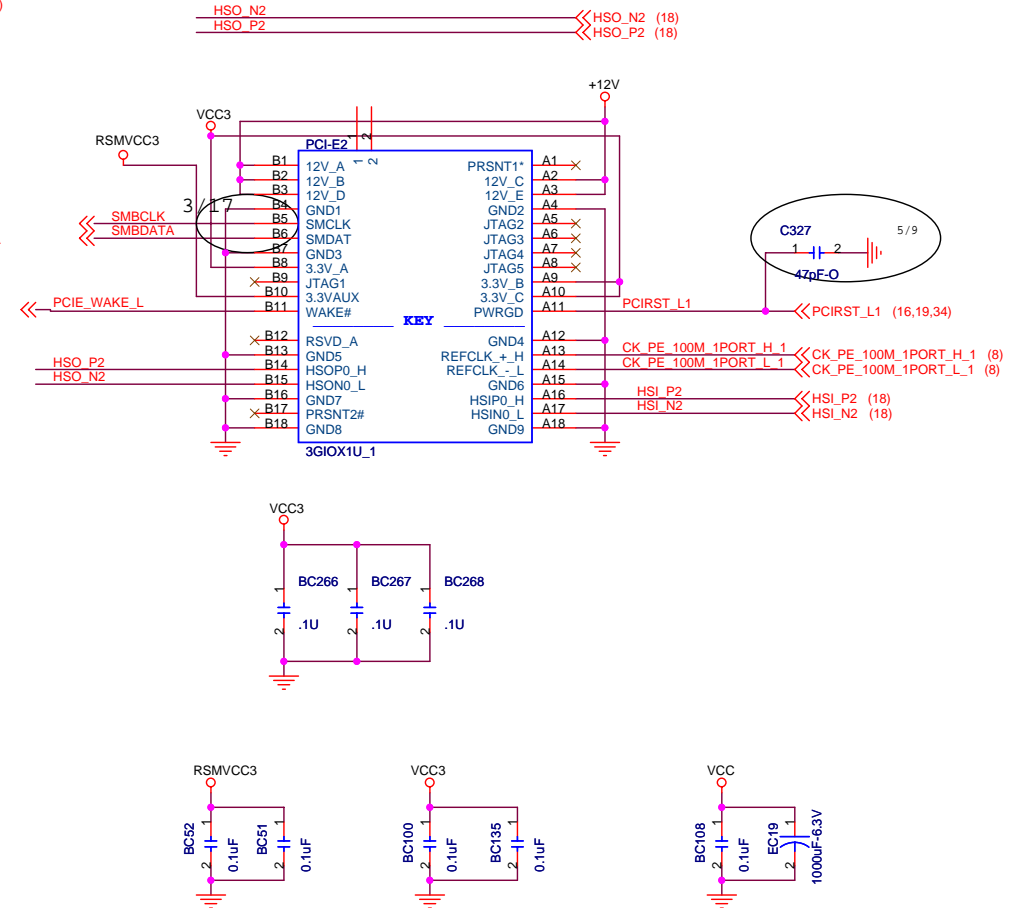
3.3V DUAL





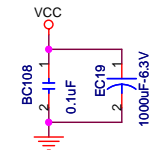
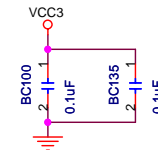
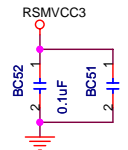
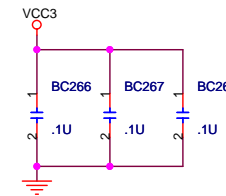
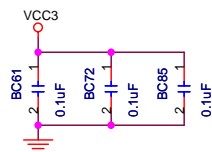


PCI Express SLOT1



PCI3-INT: IDSEL=AD19
 INTA: INTE
 INTB: INTF
 INTC: INTG
 INTD: INTH

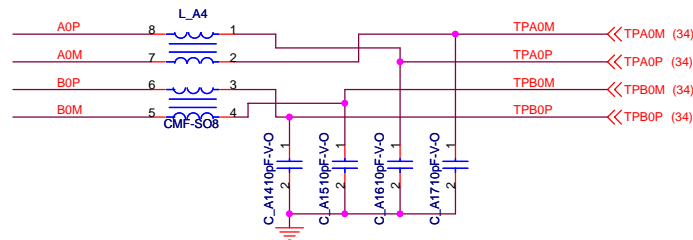
REQ=PREQ2#
 GNT=PGNT2#
 INT=INTE#



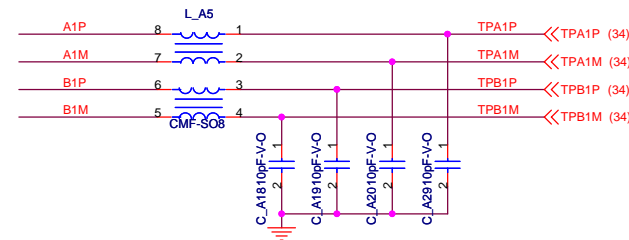
Elitegroup Computer Systems

Title		
PCI Slot 3 & PCI Extender		
Size	Document Number	Rev
Custom	945G-M6	A
Date:	Friday, November 11, 2005	Sheet 32 of 35

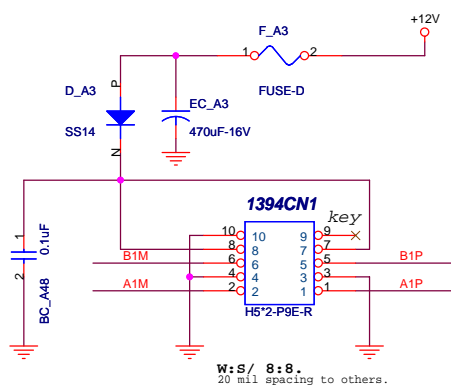
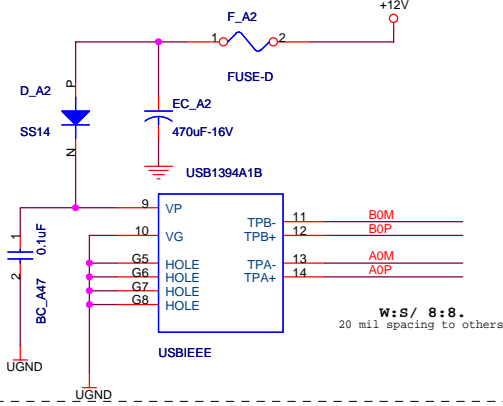
B0P	R_A90	0-0	TPB0P
B0M	R_A89	0-0	TPB0M
A0P	R_A94	0-0	TPA0P
A0M	R_A93	0-0	TPA0M



B1M	R_A92	0-0	TPB1M
B1P	R_A91	0-0	TPB1P
A1M	R_A96	0-0	TPA1M
A1P	R_A95	0-0	TPA1P



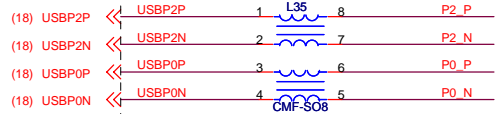
10/26



MXDIP_0	R_A97	4.7K-04	MDIP_0 (28)
MXDIN_0	R_A98	4.7K-04	MDIN_0 (28)
MXDIP_1	R_A99	4.7K-04	MDIP_1 (28)
MXDIN_1	R_A100	4.7K-04	MDIN_1 (28)
MXDIP_2	R_A101	4.7K-04	MDIP_2 (28)
MXDIN_2	R_A102	4.7K-04	MDIN_2 (28)
MXDIP_3	R_A103	4.7K-04	MDIP_3 (28)
MXDIN_3	R_A104	4.7K-04	MDIN_3 (28)

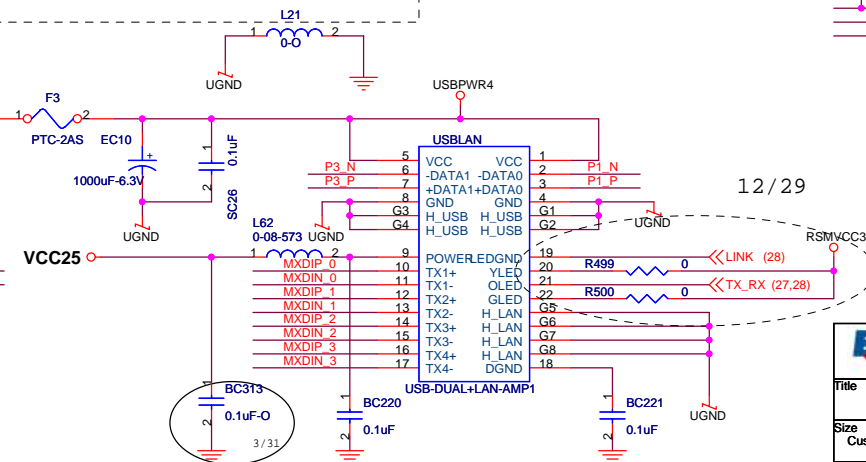
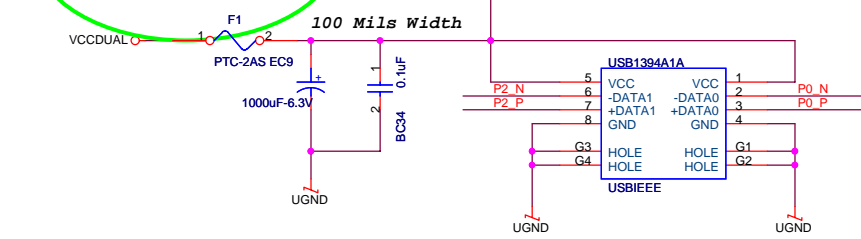
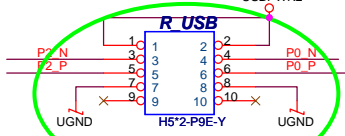
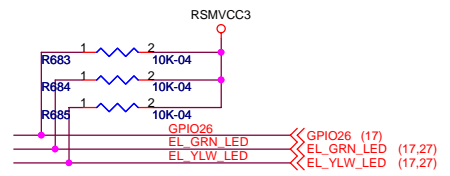
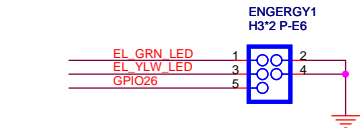
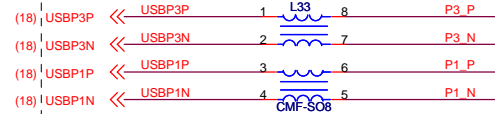
REAR_SIDE

USBP0N	R47	0-0	P0_N
USBP0P	R48	0-0	P0_P
USBP2N	R49	0-0	P2_N
USBP2P	R50	0-0	P2_P



REAR_SIDE

USBP1N	R65	0-0	P1_N
USBP1P	R62	0-0	P1_P
USBP3N	R45	0-0	P3_N
USBP3P	R42	0-0	P3_P



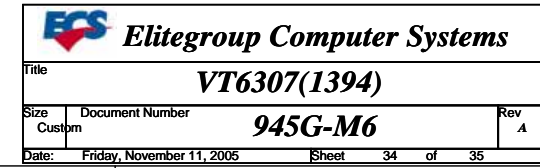
12/29

Elitegroup Computer Systems


Title: **Back I/O**

Size: Custom Document Number: **945G-M6** Rev: A

Date: Friday, November 11, 2005 Sheet: 33 of 35



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<i>Elitegroup Computer Systems</i>			
Title		 VT6307(1394)	
Size	DC	Rev	
Custom	or	945G-M6	A
Date:	Friday, November 11, 2005	Sheet	35 of 35